REMARKS

This paper is being provided in response to the Office Action dated June 14, 2006, for the above-referenced application. In this response, Applicants have cancelled claims 2, 11 and 16 without prejudice or disclaimer of the subject matter thereof and amended claims 1, 10 and 15 to clarify that which Applicants consider to be the claimed invention. Applicants respectfully submit that the amendments to the claims are fully supported by the originally-filed specification.

The objections to claims 1, 10 and 15 for informalities have been addressed by amendments contained herein in accordance with the guidelines set forth in the Office Action. Accordingly, Applicants respectfully request that this objection be withdrawn.

The rejection of claims 10-14 under 35 U.S.C. 101 as being directed to non-statutory subject matter is hereby traversed in view of the amendments to the claims contained herein. Applicants have amended the claims to recite statutory subject matter in accordance with the guidelines set forth in MPEP 2106(IV)(B)(1)(a): "[A] claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory." Accordingly, Applicants respectfully request that this rejection be withdrawn.

The rejection of claims 1, 2, 10, 11, 15 and 16 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,761,705 to DeKoning, et al. (hereinafter "DeKoning") and the

rejections of claims 3-9, 12-14 and 17-20 under 35 U.S.C. 103(a) as being unpatentable over DeKoning are hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein. Applicants have cancelled herein claims 2, 11 and 16 and incorporated the subject matter thereof into the corresponding independent claims.

Independent claim 1, as amended herein, recites a method of handling a faulting memory of a pair of mirrored memories. The method includes initially causing a non-faulting memory of the pair of mirrored memories to service all read and write operations for the pair or mirrored memories. It is determined that the hardware corresponding to the faulting memory of the pair of mirrored memories has been successfully replaced to provide a new memory. In response to the new memory being provided, data is caused to be copied from the non-faulting memory to the new memory while data is being read from and written to the non-faulting memory. In response to a write being performed to the non-faulting memory while data is being copied from the non-faulting memory to the new memory, the write is caused to be performed to the non-faulting memory and the new memory. In response to successfully copying to the new memory, writes are caused to be performed to both memories of the pair of mirrored memories and one of the pair of mirrored memories is selected for read operations when one or more read operations are performed. Claims 3-9 depend directly or indirectly from independent claim 1.

Independent claim 10, as amended herein, recites computer software, provided in a computer-readable medium, that handles a faulting memory of a pair of mirrored memories. The software includes executable code that initially causes a non-faulting memory of the pair of mirrored memories to service all read and write operations for the pair of mirrored memories.

Executable code determines that the hardware corresponding to the faulting memory of the pair of mirrored memories has been successfully replaced to provide a new memory. Executable code causes data to be copied from the non-faulting memory to the new memory while data is being read from and written to the non-faulting memory after the new memory being provided. Executable code, that in response to a write being performed to the non-faulting memory while data is being copied from the non-faulting memory to the new memory, causes the write to be performed to the non-faulting memory and the new memory. Executable code causes writes to be performed to both memories of the pair of mirrored memories and one of the pair of mirrored memories is selected for read operations when one or more read operations are performed in response to successful copying to the new memory. Claims 12-14 depend directly or indirectly from independent claim 10.

Independent claim 15, as amended herein, recites a data storage device including a plurality of disk drives, an internal volatile memory and a plurality of directors coupled to the memory. Some of the directors are coupled to the disk drives and some of the directors allow external access to the data storage device. Each of the directors handles a faulting memory of a pair of mirrored memories by initially causing a non-faulting memory of the pair of mirrored memories to service all read and write operations for the pair of mirrored memories. It is determined that the hardware corresponding to the faulting memory of the pair of mirrored memories has been successfully replaced to provide a new memory. In response to the new memory being provided, data is caused to be copied from the non-faulting memory to the new memory while data is being read from and written to the non-faulting memory. In response to a write being performed to the non-faulting memory while data is being copied from the non-

faulting memory to the new memory, the write is caused to be performed to the non-faulting memory and the new memory. In response to successfully copying to the new memory, writes are caused to be performed to both memories of the pair of mirrored memories and one of the pair of mirrored memories is selected for read operations when one or more read operations are performed. Claims 17-20 depend directly or indirectly from independent claim 15.

The DeKoning reference discloses methods and structure for maintaining cache consistency in a RAID controller having redundant caches. FIG. 1 of DeKoning shows two redudant disk array controllers (RDAC) 118.1 and 118.2 each having a cache memories 116.1 and 116.2. In dual-active RDAC pair mode, each of the pair of RDACs 118.1 and 118.2 is active in parallel with the other to maintain cache information in its own cache as well as the cache of the alternate RDAC. (See col. 5, lines 38-45 of DeKoning.) If mirrored operation is enabled then the caches 116.1 and 116.2 of the RDACS 118.1 and 118.2 must be synchronized before mirrored operation can begin. (See col. 7, lines 39-41 of DeKoning.) Each RDAC cache memory includes a battery subsystem to maintain the validity of the associated cache memory and includes a sense capability to indicate that the battery subsystem has failed at some time. (See col. 6, lines 47-61 of DeKoning).

In DeKoning's system, if the cache of one RDAC becomes invalid or "bad" a write-though mode is initiated in which all write I/O requests are immediately posted to the disk array 108 of the RAID subsystem. DeKoning distinguishes his device from the prior art by stating that, unlike prior designs that halted all operation of the RAID subsystem to await initialization/sychronization of the redundant controller caches, DeKoning's system permits

degraded operation *in write-through mode* while the caches of the dual controllers are synchronized. (See col. 9, lines 32-46 of DeKoning).

Applicants independent claims recite systems and methods for handling a faulting memory of a pair of mirrored memories that includes at least the features of providing a new memory, in response to the new memory being provided, causing data to be copied from the non-faulting memory to the new memory while data is being read from and written to the non-faulting memory, and in response to a write being performed to the non-faulting memory while data is being copied from the non-faulting memory to the new memory, causing the write to be performed to the non-faulting memory and the new memory. Specifically, Applicants provide for a system that adapts to a memory failure for operation with a minimum of disruption, but that also minimizes disruption of the back-up capability provided by mirrored memories. That is, not only does Applicants' system continuously operate in the event of memory failure, it further quickly reestablishes mirroring of data by in response to a write to the non-faulting memory, additionally causing the write to be performed to the non-faulting memory and the new memory while data is being copied from the non-faulting memory to the new memory.

In contrast, as noted above, DeKoning indicates that his device *requires* synchronization of the memory caches for mirrored operation, stating: "If mirrored operation is enabled then the caches 116.1 and 116.2 of the RDACS 118.1 and 118.2 must be synchronized before mirrored operation can begin." (See col. 7, lines 39-41 of DeKoning). In the event that the memories are not synchronized, that is one of memories is "bad," DeKoning's device provides for operation of the system, but in a "degraded" condition while the memory caches are being synchronized, in
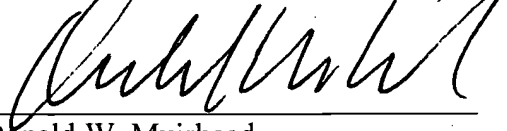
which the system operates *in a write-through mode* where all write I/O requests are immediately posted to the disk array 108 of the RAID subsystem, rather than to the memory caches. (See Fig. 1 and col. 9, lines 32-46 of DeKoning).

Accordingly, Applicants respectfully submit that DeKoning does not teach or fairly suggest at least the features of handling a faulting memory of a pair of mirrored memories, wherein *in response to a write being performed to the non-faulting memory while data is being copied from the non-faulting memory to the new memory, causing the write to be performed to the non-faulting memory and the new memory*, as claimed by Applicants. In view of the above, Applicants respectfully request that the rejections be reconsidered and withdrawn.

Based on the above, applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 508-898-8603.

Respectfully submitted,
MUIRHEAD AND SATURNELLI, LLC

Date: <u>September 12, 2006</u>

Donald W. Muirhead
Registration Number 33,978

Muirhead and Saturnelli, LLC
200 Friberg Parkway, Suite 1001
Westborough, MA 01581
(508) 898-8601 (main)
(508) 898-8602 (fax)